REMARKS

Claims 1-20 are pending in the application. Claims 1, 2 16 – 19 are rejected and claims 3-12 and 20 are objected to. Claims 13-15 have been canceled. Claims 16 and 17 have been amended. Claims 1 and 16 are independent claims.

Applicants wish to thank the examiner for indicating that dependent claims 3-12 and 20 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. At this time applicants elect not to follow the examiner's suggested course of action as the applicants believe that the claims as currently present are patentable based upon the comments below.

Independent claim 16 has been amended to incorporate the limitation of a judgment unit contained in dependent claim 17. The limitation has been deleted from dependent claim 17. No new matter has been added.

Claims 1, 2, 16 – 19 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Dimmick et al. (US 6,623,188). In response, applicants request reconsideration of this ground of rejection of the base claims based upon the amendment to the base claim and the following comments.

Claim 1 and amended 16 now recite a precoder comprising, *inter alia*, **a judgment unit for judging whether an odd number or even number of '1's exist in data input signals of N channels inputted at an n^{th} time of channel input**.

In contrast, Dimmick discloses a feed-back, parallel precoder as illustrated in FIG. 6. As applicants interpret Dimmick's circuit, it contains eight (8) D flip flops and four (4) XOR gates and four (4) buffers which do not function as a judgment unit as disclosed in the base claims.

To demonstrate the fact that Dimmick does not disclose judgment unit applicants provided a truth table, set forth in Table 1.0 representing the logical operation carried out in the circuit shown in Dimmick FIG. 6 between inputs d^0- d^3 and outputs c^0-c^3

Table 1.0

d^0	d^1	d^2	d^3	c^0	c^1	c^2	c^3	Dec value
0	**0**	**0**	**0**	**1**	**1**	**1**	**1**	15
0	0	0	1	0	1	0	0	4
0	0	1	0	1	0	0	1	9
0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	8
0	1	0	0	1	1	0	1	13

Table 1.0 was constructed under the assumption that first XOR gate in Dimmick FIG. 6 is initially set with a '0' from the feed-back output of the bottom D flip flop 468 (Q). As can be seen in Table 1.0, when the number of zeros is an even number, such as when binary 0 and 3 are fed into the circuit, the outputs c^0-c^3 provide no uniform indication of that fact(whether an even number of zeros or odd number of zeros are outputted). The converse is true in applicant's circuit as seen in the second embodiment of the present invention illustrated in FIG. 9 and discussed in the specification on page 9 – 10. To further illustrate the present invention's judgment unit applicants provide Table 2.0 below which represents the logical operations carried out in the present inventions feed-forward parallel precoder containing a judgment unit.

Table 2.0

				Judgment Unit
In1	In2	In3	In4	Output of XOR3
0	**0**	**0**	**0**	**0**
0	0	0	1	1
0	0	1	0	1
0	**0**	**1**	**1**	**0**
0	1	0	0	1

The present invention as seen in Table 2.0 and set forth in FIG. 9, provides 'XOR gate 3' which outputs a '0' when there are an even number of zeros and a '1' when there is an odd number (see specification page 9, line 8-10). Applicants content that no such logical operation

is disclosed in Dimmick circuit for judging **whether an odd number or even number of '1's exist in data input signals of N channels inputted at an n^{th} time of channel input** as recited in the rejected base claims.

Therefore, Dimmick fails to anticipate the precoder disclosed in the present invention comprising **a judgment unit for judging whether an odd number or even number of '1's exist in data input signals of N channels inputted at an n^{th} time of channel input** as recited in the base claims. Applicants respectfully request withdrawal of this ground of rejection.

The other claims in this application are each dependent from the independent claim discussed above and are therefore believed patentable for the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual consideration of the patentability of each on its own merits is respectfully requested.

For all the foregoing reasons, it is respectfully submitted that all of the present claims are patentable in view of the cited reference. A Notice of Allowance is respectfully requested.

Respectfully submitted,

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